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EXAMINER	
GERSTL, SHANE F	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/733,597	Applicant(s) BALMER ET AL.
	Examiner Shane F Gerstl	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/08/2000, 03/26/01, 01/27/03, 03/06/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *1,8 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/08/2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-16 have been examined.

Papers Received

2. Receipt is acknowledged of Oath and Declaration, Information Disclosure Statement and Foreign Priority papers submitted, where the papers have been placed of record in the file.

Specification

3. The headings of each section should not be underlined or in boldface type as described in 37 CFR 1.77(c).

The abstract of the disclosure is objected to because it exceeds 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1 and 11 are objected to because of the following informalities: lines 21 and 26 make mention of a second operand input and a second output respectively. Though the examiner is taking the term "second" to be a name for the input and output based on the specification, it is not clear if there are multiple outputs being specified for the second functional unit group based on the claim language. The examiner suggests that the input and output of reference here be labeled simply as "an operand input" and "an output" since they are connected to different circuits than that which the first operand input and first output are connected to. The examiner also asks that each

subsequent reference to these items be edited. Also, when describing the mutiplexer, it is unclear whether the comparator or multiplexer is being referred to as "having a first input receiving data..." in line 36-37. The examiner is taking the inputs and output specified here to be that of the multiplexer based on the specification. These are just examples for claim 1, however, the same objections apply to claim 11.

5. Claim 8 is objected to because of the following informalities: lines 3 and 10 refer to a third comparator and a third register file bypass multiplexer respectively. The examiner is treating the term third to simply be the name of the elements, however, using the term "third" implies a second instance of the elements. The second instance identified by the applicant is in an unrelated claim that bears no dependence on or for the current claim. The examiner suggests that the numerical identifier be removed as well as all subsequent references to it be edited.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Examiner action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1 and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor (6,266,766) in view of Hennessy (Computer Architecture).

8. In regard to claim 1, O'Connor discloses a data processing apparatus comprising:

a. a register file (figure 1, 30) comprising a plurality of registers, each of said plurality of registers having a corresponding register number; In column 3, lines 37-39 show that there are register addresses and this means that there are multiple registers within the register file and a number to specify each.

a first functional unit (figure 1, 10) connected to said register file, said first functional unit responsive to an instruction to

i. receive data from one of said plurality of registers corresponding to an instruction-specified first operand register number at a first operand input, Figure 1 shows that the functional unit receives at a first operand input data from the register file through a first operand register number (address, as shown above) and through the multiplexer (12).

ii. operate on said received data employing an instruction specified one of said first functional units, Column 2, lines 19-20 show that the functional unit outputs a result showing that it is operating on the data.

iii. output data to one of said plurality of registers corresponding to an instruction-specified first destination register number from a first output; Figure 1 shows that the output of the functional unit is written back to the register file to a register specified by a register number (address, as shown above).

a second functional unit (figure 1, 20) connected to said register file, said second functional unit responsive to an instruction to

i. receive data from one of said plurality of registers corresponding to an instruction-specified second operand register number at a second operand input, Figure 1 shows that the functional unit receives at an operand input data from the register file through another operand register number (address, as shown above) and through the multiplexer (22).

ii. operate on said received data employing an instruction-specified one of said second functional units, Column 2, lines 20-22 show that the functional unit outputs a result showing that it is operating on the data.

iii. output data to one of said plurality of registers corresponding to an instruction-specified second destination register number from a second output; Figure 1 shows that the output of the functional unit is written back to the register file to a register specified by another register number (address, as shown above).

a first comparator (figure 2) receiving an indication of said first operand register number of a current instruction and an indication of said second destination register number of an immediately preceding instruction, said first comparator indicating whether said first operand register number of said current instruction matches said second destination register number of said immediately preceding instruction (using figure 2, 60); Column 2, line 61 – column 3, line 12 gives the explanation of the comparison circuit of figure 2. The figure shows that the circuit receives an input for the current operand register number (address) and compares for a match with a second previous instruction destination register

number (result return data path 26 register address) from the second functional unit (figure 1, 20). One can see that the path, 26, is indeed the feedback path from functional group two in figure 1.

a first register file bypass multiplexer (figure 1, 12) connected to said register file (30), said first functional unit group (10), said second functional unit (20) and said first comparator (figure 2) having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said second output of said second functional unit and an output supplying an operand to said first operand input of said first functional unit group (all shown in figure 1), said first multiplexer selecting said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and selecting said second output of said second functional unit if said first comparator indicates a match. In column 2, lines 52-56, O'Connor shows that each multiplexer receives signals from a bypass control comparator circuit similar to that of figure 2. In column 3, lines 10-12, it is shown that if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit which will then select the data from the functional unit.

b. O'Connor does not disclose that the functional units are functional unit groups including a plurality of functional units.

c. Hennessy has taught on page 188 the use of functional unit groups each including a plurality of functional units. Functional unit group 1, the integer unit, contains functional units for load, store, ALU, and branch operations. Functional unit group 3, the FP adder, contains functional units for floating point add, subtract, and conversion. The other two functional unit groups contain a functional unit for each of floating point and integer multiply or divide operations.

d. The multiple functional unit groups allow for more instructions to be executed in parallel because each functional unit group contains multiple functional units. By executing more instructions in parallel, a higher pipeline throughput is achieved and thus making the processor faster.

e. The ability to speed up operation of the processor would have motivated one of ordinary skill in the art to use multiple functional unit groups in the design of O'Connor.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor to use multiple functional unit groups as disclosed by Hennessy in order to speed up the processor.

9. In regard to claim 5, O'Connor in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 1, as described above, said first comparator (figure 2) further receiving an indication of said first destination register of said immediately preceding instruction (figure 2, result return data path 16 register address), said first comparator further indicating whether said first operand register number of said current instruction matches said first destination register number of said

immediately preceding instruction (using figure 2, 50), said first multiplexer further having a third input connected to said first output of said first functional unit group (figure 1, 12), and said first multiplexer selecting said first output of said first functional unit group if said first comparator indicates a match. Just as above, the comparator checks if the first destination register address matches the current operand source address. The first functional group output is selected if the register addresses do indeed match as described above.

10. In regard to claim 6, O'Connor in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 1, as described above, said first functional unit group further responsive to an instruction to receive data from one of said plurality of registers corresponding to an instruction-specified third operand register number at a third operand input; The second input of the functional group (10) receives data from another register number through the multiplexer as shown in figure 1.

said apparatus further comprising:

a. a second comparator receiving an indication of said third operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said second comparator indicating whether said third operand register number of said current instruction matches said second destination register number of said immediately preceding instruction (using figure 2, 60); As described above, each multiplexer receives signals from a bypass control comparison circuit and thus with the addition of the multiplexer below, there is another comparator associated

with it. As described above, the circuit compares the register address of the current instruction with the second destination address.

b. a second register file bypass multiplexer (figure 1, 14) connected to said register file, said first functional unit group, said second functional unit group and said second comparator having a first input receiving data from said register corresponding to said third operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said third operand input of said first functional unit group (all shown in figure 1), said second multiplexer selecting said data from said register corresponding to said third operand number of said current instruction if said second comparator fails to indicate a match and selecting said second output of said second functional unit group if said second comparator indicates a match. As described above if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit, which will then select the data from the functional group.

11. In regard to claim 7, O'Connor in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 6, as described above,

a. said first comparator further receiving an indication of said first destination register of said immediately preceding instruction (figure 2, result return data path 16 register address), said first comparator further indicating whether said first operand register number of said current instruction matches said first destination

register number of said immediately preceding instruction (using figure 2, 50), said first multiplexer further having a third input connected to said first output of said first functional unit group (figure 1, 12), said first multiplexer selecting said first output of said first functional unit group if said first comparator indicates a match (done in same way as when the other bypass path is selected);

b. said second comparator further receiving an indication of said first destination register of said immediately preceding instruction (figure 2, result data path 16 register address), said second comparator further indicating whether said third operand register number of said current instruction matches said first destination register number of said immediately preceding instruction(using figure 2, 50), said second multiplexer further having a third input connected to said first output of said first functional unit group (figure 1, 12), and said second multiplexer selecting said first output of said first functional unit group if said second comparator indicates a match (done in same way as when the other bypass path is selected).

12. In regard to claim 8, O'Connor in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 1, as described above, further comprising:

a. a third comparator receiving an indication of said second operand register number of a current instruction and an indication of said second destination register number of said immediately preceding instruction, said third comparator indicating whether said second operand register number of said current

instruction matches said second destination register number of said immediately preceding instruction (using figure 2, 60); As described above, each multiplexer receives signals from a bypass control comparison circuit and thus with the addition of the multiplexer below, there is another comparator associated with it. As described above, the circuit compares the register address of the current instruction with the second destination address.

b. a third register file bypass multiplexer (figure 1, 22) connected to said register file, said first functional unit group, said second functional unit group and said third comparator having a first input receiving data from said register corresponding to said second operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said third operand input of said first functional unit group (all shown in figure 1), said second multiplexer selecting said data from said register corresponding to said second operand number of said current instruction if said second comparator fails to indicate a match and selecting said second output of said second functional unit group if said third comparator indicates a match. As described above if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit, which will then select the data from the functional group.

13. In regard to claim 9, O'Connor in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 8, as described above, said third

comparator further receiving an indication of said first destination register number of an immediately preceding instruction (figure 2, result return data path 16 register address), said third comparator indicating whether said second operand register number of said current instruction matches said first destination register number of said immediately preceding instruction (using element 60), said third multiplexer further having a third input connected to said first output of said first functional unit group (shown in figure 1, 22), and said third multiplexer further selecting said first output of said first functional unit group if said third comparator indicates a match (using the generated comparison signal).

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Hennessy (Computer Architecture), as applied to claims 1 and 5-9 above, and further in view of McCullough (5,826,069).

15. In regard to claim 2,

a. O'Connor in view of Hennessy discloses the data processing apparatus of claim 1, wherein said register file, said first functional unit group, said second functional unit group, said first comparator and said first register file bypass multiplexer operate according to an instruction pipeline

b. O'Connor in view of Hennessy does not disclose

i. a first pipeline stage consisting of a register read operation from said register file and a first half of operation of a selected functional unit of said first and said second functional unit groups, and

ii. a second pipeline stage consisting of a second half of operation of said selected functional unit of said first and said second functional unit groups and a register write operation to said register file,

iii. wherein the sum of the time of said register read operation and said register write operation equals approximately the sum of the time of said first and second halves of operation of a slowest of said functional units of said first and second functional unit groups.

c. McCullough has disclosed in figure 3B and column 14, lines 38-59, a timing diagram and description of the pipeline stages in his disclosed invention. The 1st half of the first stage is shown to perform a register read operation with the register being the reorder buffer. The 2nd half of the first stage is shown to determine the guarantee bits or in other words perform an operation of a functional unit. This functional operation continues through the 1st half of the second stage. The 2nd half of the second stage performs the operations necessary of a register write operation.

d. As stated in the McCullough's abstract, this allows for stores to a register file to occur within one clock cycle and thus save time. This quick storage into the register file would have motivated one of ordinary skill in the art to modify the disclosure of O'Connor in view of Hennessy to include the pipeline makeup given by McCullough.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Hennessy to have the pipeline stage makeup given by McCullough in order to achieve quick stores to the register file.

16. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Hennessy (Computer Architecture), as applied to claims 1 and 5-9 above, and further in view of Olson (5,123,108).

17. In regard to claim 3,

a. O'Connor in view of Hennessy discloses the data processing apparatus of claim 1, as described above, wherein said first comparator further receives an indication of said second destination register number of a second preceding instruction (figure 2, result return data path 26 register address), said first comparator further indicating whether said first operand register number of said current instruction matches said second destination register number of said second preceding instruction (using figure 2, 60), and wherein said multiplexer further has a third input (figure 1, 12).

b. O'Connor in view of Hennessy does not disclose that the apparatus is further comprising an output register having an input connected to output of functional unit group and an output connected to said register file for temporarily storing said output of said second functional unit group prior to storing in said register corresponding to said destination register number, wherein said multiplexer has an input connected to said output register output, said multiplexer selecting said output register output if said first comparator indicates a match.

c. Olson discloses a data processing apparatus with register bypassing (figure 2) further comprising an output register (figure 2, 28a) having an input connected to the output of the functional unit and an output connected to said register file for temporarily storing said output of function unit prior to storing in said register corresponding to said destination register number (address), wherein multiplexer (figure 2, 18) has an input connected to said output register output, said multiplexer selecting output register output if comparator (figure 2, 24) indicates a match (column 4, lines 6-16).

d. The output register given by Olson has numerous desirable qualities. First, one can be sure that the correct data is being written to the register file because the output register will hold the data throughout the clock cycle. Also, using the register in conjunction with the disclosure of O'Connor allows for the retention of preceding data for another clock cycle which is used by the multiplexer on a third input for extended bypassing capabilities.

e. This increased data integrity for the register file and the ability to have more data readily available for bypassing purposes would have motivated one of ordinary skill in the art to incorporate the teaching of Olson's output register into the design of O'Connor in view of Hennessy.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Hennessy to include the output register specified by Olson in order to have high data integrity in the register file and to have more data available for register bypassing purposes.

18. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Hennessy (Computer Architecture) further in view of Olson as applied to claim 3 above, further in view of Lai (6,382,846), and further in view of Hennessy (Computer Organization).

19. In regard to claim 4, O'Connor in view Hennessy further in view of Olson discloses

a. the data processing apparatus of claim 3, wherein said register file, said first functional unit group, said second functional unit group, said first comparator, said first register file bypass multiplexer, and said output register operate according to an instruction pipeline (O'Connor, column 1, lines 60-61)

b. O'Connor in view Hennessy further in view of Olson does not disclose

i. a first pipeline stage consisting of a register read operation from said register file;

ii. a second pipeline stage consisting of an operation of a functional unit; and

iii. a third pipeline stage consisting of a register write operation to said register file,

iv. wherein the time of said register read operation and the time of said register write operation are each equal approximately to the time of operation of a slowest of said selected functional units of said first and second functional unit groups.

c. Lai has disclosed in column 1, lines 50-51 the use of a register read stage, an execution stage, and a post-execution register write stage. Hennessy has disclosed on page 452, bottom paragraph, that all instructions advance during each clock cycle from one pipeline register to the next. Since it is inherent that the clock cycle is constant, this means that each stage takes the same amount of time to complete.

d. Lai has taught in column 1, lines 63-66, that a register read stage provided in processors with a register file allows for quick and efficient retrieval of information in the register file. The execution stage is standard in a pipeline processor for performing operations on the data. Lai has also taught in column 2, lines 2-4 that the register write stage quickly and efficiently stores values in the register file. By having each pipeline stage the same length, the control of the processor becomes incredibly simpler.

e. The ability to read from and write to the register file in a quick and efficient manner and so that the processor executes needed operations in a single cycle all while keeping control simple by having each stage of the same length would have motivated one of ordinary skill in the art to use the design of Lai and Hennessy with the design of O'Connor in view of Hennessy further in view of Olson.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Hennessy further in view of Olson to include the designs of Lai and Hennessy so that reads from and writes to the register are quick

and efficient and so the processor executes needed operations in a single cycle all while keeping control simple.

20. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Hennessy (Computer Architecture) as applied to claims 1 and 5-9 above, further in view of Kawasaki (5,467,476) and further in view of Hennessy (Computer Architecture).

21. In regard to claim 10,

a. O'Connor in view of Hennessy discloses: the data processing apparatus of claim 1, as described above,

b. O'Connor in view of Hennessy does not disclose the apparatus further comprising a third functional unit group connected to said register file, wherein said third functional unit group's register file output data is available for register file bypass solely within the third functional unit group itself.

c. Hennessy has taught on page 188 the use of four functional unit groups (which also comprises three). The examiner is taking official notice that it is well known in the art that the more functional units exist, the more instructions can be executed simultaneously and thus the pipeline will have a greater throughput. Kawasaki has shown in figure 2 the use of bypass in the functional units solely within that functional unit itself. This simplifies the control of the bypass unit since the functional unit will only send its output to itself and not the other functional units.

d. This ability to increase pipeline throughput as well as simplify bypass control would have motivated one of ordinary skill in the art to incorporate a third functional unit group as shown in Hennessy as well as allow bypassing in the third functional unit group solely to itself as shown by Kawasaki into the design of O'Connor in view of Hennessy.

It would have been obvious to one of ordinary skill in the art to modify the design of O'Connor in view of Hennessy to include a third functional unit group as shown by Hennessy and to use bypassing from this group solely to itself so as to increase pipeline throughput and simplify bypass control.

22. Claim 11, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Deao (5,970,241) and further in view of Hennessy (Computer Architecture).

23. In regard to claim 11,

a. O'Connor discloses a data processing apparatus comprising:

i. a first register file (figure 1, 30) comprising a plurality of registers, each of said plurality of registers having a corresponding register number; In column 3, lines 37-39 show that there are register addresses and this means that there are multiple registers within the register file and a number to specify each.

ii. a first functional unit group (figure 1, 10) including an input connected to said register file, an output connected to said register file,

and a plurality of first functional units, said first functional unit group responsive to an instruction to

(1) receive data from one of said plurality of registers in said register file corresponding to an instruction-specified first operand register number at a first operand input; Figure 1 shows that the functional unit group receives at a first operand input data from the register file through a first operand register number (address) and through the multiplexer (12).

(2) operate on said received data employing an instruction specified one of said first functional units; Column 2, lines 19-20 show that the functional unit group outputs a result showing that it is operating on the data.

(3) output data to one of said plurality of registers in said register file corresponding to an instruction specified first destination register number from a first output; Figure 1 shows that the output of the functional unit group is written back to the register file to a register specified by a register number (address).

iii. a second functional unit group (figure 1, 20)including an input connected to said register file, an output connected to register file, and a plurality of second functional units, said second functional unit group responsive to an instruction to

(1) receive data from one of said plurality of registers in said register file corresponding to an instruction-specified second operand register number at a second operand input; Figure 1 shows that the functional unit group receives at an operand input data from the register file through another operand register number (address) and through the multiplexer (22).

(2) operate on said received data employing an instruction specified one of said second functional units; Column 2, lines 19-20 show that the functional unit group outputs a result showing that it is operating on the data.

(3) output data to one of said plurality of registers in said register file corresponding to an instruction-specified second destination register number from a second output; Figure 1 shows that the output of the functional unit group is written back to the register file to a register specified by another register number (address).

iv. a first path connecting said register file to first functional unit group comprising

(1) a first comparator (figure 2), wherein, said comparator receives an indication of said first operand register number of a current instruction and an indication of said second destination register number of a preceding instruction, and said first crosspath

comparator indicates whether said first operand register number of said current instruction matches said second destination register number of said preceding instruction (using figure 2, 60); Column 2, line 61 – column 3, line 12 gives the explanation of the comparison circuit of figure 2. The figure shows that the circuit receives an input for the current operand register number (address) and compares for a match with a second previous instruction destination register number (result return data path 26 register address) from the second functional unit (figure 1, 20). One can see that the path, 26, is indeed the feedback path from functional group two in figure 1.

(2) a first multiplexer (figure 1, 12) connected to said register file (30), said first functional unit group (10), said second functional unit group (20) and said first comparator (figure 2) having a first input receiving data from said register corresponding to said first operand register number of said current instruction, a second input connected to said second output of said second functional unit group and an output supplying an operand to said first operand input of said first functional unit group (all shown in figure 1), wherein, said first multiplexer selects said data from said register corresponding to said first operand number of said current instruction if said first comparator fails to indicate a match and

selects said second output of said second functional unit group if said first comparator indicates a match. In column 2, lines 52-56, O'Connor shows that each multiplexer receives signals from a bypass control comparator circuit similar to that of figure 2. In column 3, lines 10-12, it is shown that if current operand register number (address) is the same as the register number (address) of the return path (previous instruction destination) then a logical one is output by the comparison circuit which will then select the data from the functional group.

b. O'Connor does not disclose

i. a second register file comprising a plurality of registers,

ii. both functional groups being connected to both register files;

iii. the first path being a crosspath where the first comparator checks if the first operand register is in the second register file.

iv. the functional units are functional unit groups including a plurality of functional units.

c. Deao has disclosed in figure 2:

i. a second register file (20b) comprising a plurality of registers;

ii. both functional groups (L1,S1,M1,D1, and L2,S2,M2,D2) being connected to both register files (by crosspaths 1x and 2x);

iii. the first path being a crosspath where the first comparator checks if the first operand register is in the second register file. Deao shows the

crosspath (1x) from the second register file (20b) where the multiplexer shown then selects the appropriate register file to select from depending on where the correct operand is.

Hennessy has taught on page 188 the use of functional unit groups each including a plurality of functional units. Functional unit group 1, the integer unit, contains functional units for load, store, ALU, and branch operations. Functional unit group 3, the FP adder, contains functional units for floating point add, subtract, and conversion. The other two functional unit groups contain a functional unit for each of floating point and integer multiply or divide operations.

d. The crosspath and second register file of Deao provides for increased quantity and flexibility in nearby available data. Having more data in local registers means quicker data access because of the close proximity and faster access time of registers. This increased quantity and flexibility of quickly accessible data would have motivated one of ordinary skill in the art to incorporate the given design of Deao for crosspaths into O'Connor.

The multiple functional unit groups allow for more instructions to be executed in parallel because each functional unit group contains multiple functional units. By executing more instructions in parallel, a higher pipeline throughput is achieved and thus making the processor faster. The ability to speed up operation of the processor would have motivated one of ordinary skill in the art to use multiple functional unit groups in the design of O'Connor.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor to include the second register file and crosspath design given by Deao as well as the multiple functional unit groups of Hennessy in order to gain greater capacity and flexibility of quickly accessible data while increasing processor speed as a whole.

24. In regard to claim 12, O'Connor in view of Deao further in view of Hennessy (Computer Architecture), as described above, discloses the data processing apparatus of claim 11 further comprising a second crosspath (Deao, figure 2, 2x) connecting said first register file to said second functional unit group.

25. In regard to claim 15, O'Connor in view of Deao further in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 11 further comprising:

a. a first input comparator receiving an indication of said first operand register number of a current instruction, said first comparator indicating whether said first operand register number is in said first register file or said second register file; This comparator is inherent because of the function of the mutiplexer described below. The multiplexer chooses which register file to retrieve data from. The only way to do this is by comparing the register number (address) of the current instruction with the range of such numbers in each register file.

b. a first input multiplexer (Deao, figure 2, 211) having a first input connected to said first register file (20a), a second input connected to said first crosspath (1x), and an output connected to said first functional unit group (L1,S1,M1,D1),

said first input multiplexer selecting said first input if said first input comparator indicates said register corresponding to said first operand number is in said first register file, and selecting said second input if said first input comparator indicates said register corresponding to said first operand number is in said second register file. It can be seen in the figure and in column 9, lines 11-13, that the multiplexer selects the data from the correct register file based on where the needed data exists.

26. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Deao further in view of Hennessy (Computer Architecture) as applied to claim 11 above, and further in view of Kawasaki (5,467,476).

27. In regard to claim 13,

a. O'Connor in view of Deao further in view of Hennessy discloses the data processing apparatus of claim 11,

b. O'Connor in view of Deao further in view of Hennessy does not disclose a first crosspath register latching said crosspath multiplexer's output.

c. Kawasaki has shown in figure 4, the use of a flip-flop register in element 141a to hold the multiplexed data for the first operand input of the functional unit. This register allows for the correct data to be latched to the functional unit on each clock cycle, insuring data integrity of all operands to be operated upon. The same technique would have the same effect in the design of O'Connor in view of Deao further in view of Hennessy. By holding the register data through each cycle, one can be sure that the correct data is operated on.

d. This data integrity would have motivated one of ordinary skill in the art to incorporate the multiplexer output latching technique used by Kawasaki in the design of O'Connor in view of Deao further in view of Hennessy and its crosspath multiplexer.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Deao further in view of Hennessy to use the multiplexer lathcing method taught by Kawasaki in order to have high data integrity.

28. Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor in view of Deao further in view of Hennessy (Computer Architecture) as applied to claim 11 above, and further in view of Hennessy (Computer Architecture).

29. In regard to claim 14,

a. O'Connor in view of Deao further in view of Hennessy discloses

the data processing apparatus of claim 11, as described above, comprising a functional unit group including an input connected to said first and second register files, an output connected to said first register file, and a plurality of functional units, said functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first and second register files corresponding to said instruction-specified first operand register number at an operand input,

operate on said received data employing an instruction specified one of said third functional units, and

output data to one of said plurality of registers in said first register file corresponding to an instruction-specified destination register number from an output,

said first crosspath further connecting said second register file to said functional unit group, and said first crosspath multiplexer further having an output supplying an operand to said operand input of said functional unit group.

All of the above as applied to claim 11.

b. O'Connor in view of Deao further in view of Hennessy does not disclose that the above is also incorporated into a third functional unit group.

c. Hennessy has disclosed on page 188 a pipeline including four functional unit groups, which consequently also comprises three functional unit groups. The examiner is taking official notice that it is well known in the art that the more functional units exist, the more instructions can be executed simultaneously and thus the pipeline will have a greater throughput. Contemporaneously, it would be advantageous to incorporate the third functional unit group given by Hennessy for use with the bypassing method disclosed by O'Connor in view of Deao in order to avoid register read times when possible.

d. The ability to increase instruction throughput would have motivated one of ordinary skill in the art to add a third functional unit group as shown by Hennessy to the design of O'Connor in view of Deao further in view of Hennessy and to

include the register bypassing technique disclosed therein with the third functional unit in order to cut register read time.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Deao further in view of Hennessy to include a third functional unit group as taught by Hennessy in order to increase pipeline throughput and to use the bypass technique of O'Connor in view of Deao further in view of Hennessy with that functional unit group in order to speed up data retrieval.

30. In regard to claim 16,

a. O'Connor in view of Deao further in view of Hennessy (Computer Architecture) discloses the data processing apparatus of claim 15, as described above, comprising a functional unit group including an input connected to said first and second register files, an output connected to said first register file, and a plurality of functional units, said functional unit group responsive to an instruction to

receive data from one of said plurality of registers in said first or second register files corresponding to an instruction specified operand register number at an operand input,

operate on said received data employing an instruction specified one of said functional units, and

output data to one of said plurality of registers in said first register file corresponding to an instruction-specified destination register number from an output,

said first input comparator further receiving an indication of said destination register number of an immediately preceding instruction, said input first comparator indicating whether said first operand register number of said current instruction matches said destination register number of said immediately preceding instruction, and

said first input multiplexer further having a third input connected to said output of functional unit group, said first multiplexer selecting said output of said functional unit group if said first input comparator indicates a match.

All of the above is applied to claim 11.

b. O'Connor in view of Deao further in view of Hennessy does not disclose the above functionality being used on a fourth functional unit group.

c. Hennessy has disclosed on page 188 a pipeline including four functional unit groups, which consequently also comprises three functional unit groups. The examiner is taking official notice that it is well known in the art that the more functional units exist, the more instructions can be executed simultaneously and thus the pipeline will have a greater throughput. Contemporaneously, it would be advantageous to incorporate the third functional unit group given by Hennessy for use with the bypassing method disclosed by O'Connor in view of Deao further in view of Hennessy in order to avoid register read times when possible.

d. The ability to increase instruction throughput would have motivated one of ordinary skill in the art to add a third functional unit group as shown by Hennessy to the design of O'Connor in view of Deao further in view of Hennessy and to

include the register bypassing technique disclosed therein with the third functional unit in order to cut register read time.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of O'Connor in view of Deao further in view of Hennessy to include a third functional unit group as taught by Hennessy in order to increase pipeline throughput and to use the bypass technique of O'Connor in view of Deao further in view of Hennessy with that functional unit group in order to speed up data retrieval.

Conclusion

31. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to register bypassing in general.

US Pat No 5,619,668 to Zaidi shows the use of register bypassing for multiple operands with selection control and an output feedback latch.

US Pat No 5,043,868 to Kitamura shows the use of register bypassing based on the result of a comparison circuit

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
October 27, 2003

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